Solicitation For ASIC Foundry Services

5/7/2001

Introduction:
The National Polar-orbiting Operational Environmental Satellite System (NPOESS) Integrated Program Office (IPO) requires ASIC foundry services for its radiation-hardened high-speed data bus ASIC effort. The high speed data bus will implement a 1394a-2000 S100 OCHI compliant high performance serial bus operating at 100 Mbps which will interface to onboard processors (CPUs) using a Compact Personal Computer Interface (cPCI). The ASICs will be used on instruments aboard the NPOESS satellites.

The rapid ASIC development and fabrication requires early form, fit and function 1394a-2000 ASIC rad-hard parts to support the development of several NPOESS instruments currently in design. The IPO prefers a supplier with proven radiation hardened processes that have produced ASICs with demonstrated long on-orbit space operations. The technology used should be a low risk, highly mature process with space flight history; state-of-the art technologies (i.e. technologies with geometries smaller than 0.5 μ) are not preferred unless qualified by actual on-orbit, long term space operations. The supplier must have an entry point into their process to use government furnished design files (EDIF netlist, test vectors, and GDSII) in the production of the ASICs.

Description:
The IPO design team is incorporating the 1394a-2000 OHCI and cPCI intellectual property (IP) procured from InSilicon (San Jose, CA) as the baseline cores for the design. In agreement with InSilicon, the IPO will assign the IP to the supplier selected from this combined synopsis/solicitation for the project's duration; thus, the supplier is not required to purchase IP from InSilicon for this effort. The InSilicon cores are Verilog so all design files supplied to the supplier shall be Verilog, not VHDL. Three ASICs shall be developed under this 1394a-2000 effort. The two digital ASICs shall use standard gate array products and the one analog ASIC shall require a full custom ASIC. All ASICs shall be packaged in hermetic ceramic quad flat packs (CQFP). Packaging shall be the responsibility of the supplier with agreement of the IPO and any IPO agent assisting with the 1394a-2000 design. All synthesis and test vectors supplied to the supplier will have been implemented in Synopsis on Sun UltraSPARC workstations. The following summarizes estimated requirements:

1. The 1394a-2000 Link Layer Controller (LLC) and Compact PCI (cPCI) interface ASIC shall require approximately 150K gates and require a 172-pin (TBR) CQFP. This part shall include three 2 Kbyte FIFOs (or Dual Port RAM) with an SEU < 1e-8 errors/bit-day and approximately 1500 flip flops with SEU < 1e-10 errors/bit-day. The ASIC shall be immune to SEL and radiation hardened to at least 100 krad TID. This ASIC must support a 33 MHz cPCI interface and a 50 MHz Media interface to the digital physical layer (DPHY) chip. An EDIF netlist and test vectors will be provided to the supplier.
2. The 1394a-2000 Digital Physical Interface (DPHY) ASIC includes most of the digital circuitry of the 1394a-2000 Physical Layer (PHY). It shall require approximately 50K

gates and a 132-pin (TBR) CQFP. This part shall include approximately 1500 flip-flops with SEU < 1e-10 errors/bit-day. The ASIC shall be immune to SEL and radiation hardened to at least 100 krad TID. It must support a 50 MHz Media interface with the LLC ASIC and a 50 MHz PHY interface to the analog physical layer (APHY) chip. Again, an EDIF netlist and test vectors will be provided to the supplier.

3. The 1394a-2000 Analog Physical Layer (APHY) ASIC includes the analog circuitry of the 1394a-2000 PHY Layer. This design will be a full custom analog ASIC packaged in a 64-pin (TBR) CQFP. The ASIC shall be immune to SEL and radiation hardened to at least 100 krad TID. It shall interface with the DPHY via the 50 MHz PHY interface and provide the 50MHz internally clocked S100 Firewire interface, requiring 100 Mbps transceivers compliant with the 1394a-2000 specification. This design shall provide the supplier with GDSII graphics files and test methodology for chip verification.

Delivery:

Since the 1394a-2000 design effort is schedule critical, proposals demonstrating time-accelerated, expeditious production capabilities and on-time or better deliveries of the parts will receive better ratings for the schedule evaluation. Proposers should substantiate on-time delivery claims with past programs. NPOESS IPO requests points-of-contact of these past programs as a follow up to the company's claims.

Proof-of-Design Parts -

Due to the mission critical nature of the 1394a-2000 ASIC development, production and delivery of Proof-of-Design (POD) parts must be expedited. NPOESS is requesting no more than 12 weeks from the release of the EDIF netlists to POD delivery for the two digital ASICs and no more than 12 weeks from the release of the GDSII files to POD delivery of the analog ASIC.

Engineering & Flight Parts –

NPOESS requires engineering and flights parts to support the satellite and sensor development. Engineering parts must meet all cPCI and 1394a-2000 specifications over worst-case temperature and voltage but do not require full QML screening. The flight parts shall be produced to QML-Q and QML-V quality levels. Engineering parts are required by the project no later than March 1, 2002 to support instrument development; final QML-V flight parts must be available for later purchase and delivery by June 1, 2002 for integrating into the final flight sensors and spacecraft.

Company Qualification:

Companies responding to this combined synopsis/solicitation should have well-established radiation hardened technology and processes used in the space industry. NPOESS is more interested in a timely execution than pushing smaller geometry "state-of-the-art". Thus NPOESS is considering geometries on the order of 0.5 – 0.6 µ since these processes are very mature and have proven flight history on past space programs. Smaller geometries may be proposed if the supplier can prove flight history and meet

delivery schedules. Proposers should document how their foundry has been used in past space programs and what products have actual space flight exposure (not just "designed in" to unflown projects).

In its proposal, the proposer should address the technical risk and feasibility of its recommended process technology, and demonstrate how their process will meet or exceed the requirements and performance needs of the InSilicon IP. It is preferred, but not required, that the proposer, working directly with InSilicon, prove that their process technology will meet the performance requirements using the actual InSilicon PCI and 1394 IP. Since the cPCI and 1394a-2000 have strict timing requirements, the proposer should provide enough details to show that their product will have sufficient timing margin over worst-case conditions of temperature (-55 - +125 C), process, voltage (+/- 5%), and radiation (~30Krad), encountered in the space environment. One of the following three metrics shall be supplied to the IPO for review:

- a Synopsis timing report from the actual InSilicon IP PCI synthesis;
- a Synopsis timing report from some other design demonstrating the process is PCI compliant; or
- a timing analysis demonstrating that the processed process can meet or exceed performance requirements of PCI

The important thing here is that since the InSilicon IP is what is being designed into the ASICs, the supplier must substantiate their technology or provide simulation results with this IP so that NPOESS can be assured no production glitches will be encountered at the foundry.

In its proposal, the selected company should provide library models and foundry design rules of its proposed products to the IPO design team for the 1394a-2000. These libraries will allow the development of the commercial InSilicon IP into a radiation-hardened part for space. Foundry design rules must be provided early to assure the analog ASIC design team has proper rules to design the full custom ASIC, precluding a "false-start" using wrong design rules.

Immediate and Extended Support:

Once a foundry contractor has been selected as a result of this combined synopsis/solicitation and a contract awarded, and once files are delivered from the customer, the selected company shall provide weekly status updates addressing the progress made and the following week's tasking. These data assist the High Speed Data Bus Manager to monitor and maintain schedule on the 1394a-2000 effort. The weekly status update shall take the form of informal e-mails sent to the Data Bus Manager. As required, additional information may be requested via telephone. Therefore, the company shall also provide easy access to key personnel for timely resolution of design issues and the interchange of information. The company shall host and support design reviews (PDR and CDR) for the three ASIC parts being developed.

The NPOESS Program is a protracted mission running through 2018. Proposers must provide a plan describing continued support for the duration of the program. After initial development of the chip set by the IPO, the design shall be assigned to the supplier

selected from this combined synopsis/solicitation for long-term support. The design shall remain a wholly-owned government product. The IPO expects the supplier will make available these chipsets or qualified functionally equivalent parts which meet or exceed the 1394a-2000 S100 and to continue full technical support for the chip set until 2018.

Foundry Effort:
Excluding a preliminary design phase requiring early interaction between the IPO design team and the supplier to lay out the ground rules**,** there are four phases required for the development and fabrication of each of the ASICs. Each phase ends with a milestone which allows an opportunity for assessing the progress and viability of the ASIC foundry effort.

Phase 0 – Restating the requirement from above, immediately after award the selected company must provide library models and foundry design rules of its products to the IPO design team to allow them to develop the commercial InSilicon IP into a radiation-hardened part for space. Foundry design rules must be provided early to assure the analog ASIC design team has proper rules to design the full custom ASIC, precluding a "false-start" using wrong design rules. Gate array library models are required to design, synthesize, and simulate the digtal ASICs to verify that the cPCI interface and 1394 logic has sufficient timing margin. The supplier shall provide consulting support on their process, manufacturing, and test methods to the design team as needed.

Phase I – In Phase I, the supplier shall receive the design in the form of EDIF netlists and/or GDS II files from the NPOESS 1394a-2000 developer. Test vectors and detailed analog simulation files shall be provided so that the supplier can perform simulations on the incoming design files for design acceptance. For scheduling purposes, these files are estimated to be available no earlier than May 28, 2001 but not later than Aug 15, 2001. A preliminary design review (PDR) shall be held to assure all design information has been transferred to the supplier. The supplier then shall place and route the design and generate detailed clock trees and buffering. A post route simulation and timing analysis shall be done. Netlist and simulation design files needed for an independent design check and simulation, as well as the timing information files, shall be sent to the IPO or the IPO's agent for review and final simulation. After final verification of the design, a critical design review (CDR) shall be held to ensure that the ASIC designs meet all specifications of both the IPO and the supplier.

Phase II – In Phase II, the design is released for fabrication of the proof-of-design (POD) parts. The supplier shall design any masks or other structures to complete the metallization of the gate arrays and the full custom analog ASIC. The supplier shall fabricate and package 20 PODs of each ASIC type. During fabrication, the supplier and the IPO design team shall define a 1394a-2000 OHCI test plan for each part and the supplier shall implement this test plan for chip verification testing. Specific test structures, representing distinct pieces of the analog design, may be implemented on the analog ASIC by either the supplier or the IPO analog

ASIC design team to facilitate testing and debug of the full custom analog ASIC and for future radiation tolerance characterization. As a minimum, testing shall verify sufficient timing margin, signal integrity, and voltage drive over worst-case temperature and voltage extremes at the chip interface (i.e. pinouts). All chip verification test data shall be delivered to the IPO's ASIC design team. A review shall be held to review the test data for completeness and to ensure that the ASIC PODs physically meet all the specifications called out at the CDR. The 20 sets of PODs shall be delivered to the IPO design team for 1394a-2000 characterization and validation.

Phase III – This phase is intended as a place holder should a second pass be required for one or more of the ASICs. A second pass would be required should problems arise during the foundry chip verification or in the full up, combined ASIC verification done by the IPO design team. The IPO must plan in a second pass to fix problems or errors in improper metallization (logic or timing problems) or for poorly performing analog ASIC. Fabrication and testing would follow the details of Phase II above.

Phase IV – After full characterization and validation of the 1394a-2000 OHCI chip set by the IPO design team, Phase IV sets up fabrication and testing for full flight qualified parts – parts to QML Class Q and V. The supplier shall have current Qualified Manufacturer List (QML) certification. The supplier shall make parts available to parties associated with the NPP and NPOESS satellite programs for the duration of the programs. As stated above the supplier shall submit to the IPO a plan detailing continued support and assured supply of parts for the NPOESS contractors through 2018. Full radiation and temperature characterization shall be part of the parts qualification.

Cost Quote:

The supplier costs shall be firm fixed price. The quote should include any general contracting notes, assumptions, requirements, recommendations, and restrictions. An itemization showing responsibilties for deliverables, various development and fabrication tasks, and reviews should be provided as a check list for the IPO. All tasks, analyses, syntheses, simulations, and reviews should be explicitly called out. The proposal shall show a breakdown of non-recurring engineering (NRE) cost:

- for POD design and development which correlates with Phases 0 – IV defined above
- for package engineering
- for test engineering, test jigs and running tests (list all specific tests being quoted)
- for extended support
- for program management
- for documentation and test data/reports.

The cost per part for engineering, QML-Q, and QML-V flight parts and any optional charges shall be quoted. The proposer shall bid piece prices for lots of 25, 50, and 100 sets of the three ASIC set.

Schedule:
The proposal must clearly demark task milestones and durations. The proposal must clearly depict following tasks for the two digital gate array ASICs and the full custom analog ASIC on a schedule for comparison with the IPO 1394 Master Schedule:

- Library Models & Design Rules Available
- Design Review & Acceptance – PDR
- Place & Route Physical Design
- Post Route Synthesis, Timing Analysis, Final Timing Simulation, Formal Verification - CDR
- Final Release to Fab
- Wafer Fabrication
- Parts Testing – POD Chips Released
- QML Parts Fabrication
- Engineering (QML-Q) Testing and Availibility
- Flight (QML-V) Parts Testing and Availibility
- Documentation/Test Report Deliveries